IN THE CLAIMS:

1. (Amended) A delay locked loop for use in a semiconductor memory device, comprising:

a controllable delay chain means for controlling a delay time of a clock signal coupled thereto;

a comparison means for **[detecting the increase and decrease of the delay time by]** comparing a reference clock signal with a delayed clock signal generated from the controllable delay chain means and detecting a need for an increase or decrease of the delay time; and

an instant locking delay control means for detecting whether a locking between the reference clock signal and the delayed clock signal is accomplished, **[compensating, in response to an output signal generated from the comparison means, a locking due to a noise to thereby increasing or decreasing the delay time, and directly controlling the controllable delay chain means by using the output signal of the comparison means in case the delay time is not locked]**

wherein, when the locking is accomplished, the instant locking delay control means is operated to compensate for noise detected by the comparison means and to control the controllable delay chain means, and

wherein, when the locking is not accomplished, the instant locking delay control means is not operated to compensate for noise and the output signals generated by the comparison means are used to directly control the controllable delay chain means.

2. (Amended) The delay locked loop of claim 1, wherein the instant locking delay control means includes:

a delay controller for counting a number of times the output signal of the comparison means is activated and generating a signal **[having increasing or decreasing information of]** requesting an increase or decrease of the delay time if the counted number is larger than a predetermined value;

a locking detector for detecting, in response to the reference clock signal and the delayed clock signal, whether the **[delay time is locked or not]** locking is accomplished and generating a selection signal **[of]** representing whether the **[delay time is locked or not]** locking is accomplished; and

a shift multiplexer for selectively outputting **[either]** one of the output signal of the comparison means **[or that]** and the output signal of the delay controller in response to the selection signal, thereby controlling the controllable delay chain means.

3. The delay locked loop of claim 2, wherein the locking detector **[contains]** comprises:

a first delay unit for delaying the delayed clock signal by a predetermined time to thereby generate a delayed output signal;

a second delay unit for delaying the reference clock signal by a preset time to thereby produce a delayed reference clock signal;

a first determination unit for determining, in response to the reference clock signal and the delayed output signal, whether the delayed output signal is slower than the reference clock signal;

a second determination unit for deciding, in response to the delayed clock signal and the delayed reference clock signal, whether the delayed reference clock signal is slower than the delayed clock signal; and

a logic unit for generating the selection signal based on output signals of the first and the second determination units.

4. The delay locked loop of claim 3, wherein the locking detector further **[contains]** comprises an output unit for delaying, **[insponse]** in response to the reference clock**[s]** signal, an output signal of the logic unit when the [delay time is locked] locking is accomplished, to thereby control the shift multiplexer.

5. The delay locked loop of claim 4, wherein the output unit **[contains]** comprises:

a plurality of shift registers **[which]** configured to shift the output signal of the logic unit and **[are capable of being]** to be reset;

a NAND gate for performing a negative AND operation for shifted values of the plurality of shift registers;

and an inverter for producing the selection signal by inverting an output of the NAND gate.

6. The delay locked loop of claim 4, wherein the output unit **[contains]** comprises:

a plurality of shift registers **[for receiving]** configured to receive the output signal of the logic unit as their reset signal and [shifting] to shift a high data value input**[ted]** to [its] a first of the registers; and

an output means for generating a data value output**[ted]** from the last one of the shift registers as the selection signal.